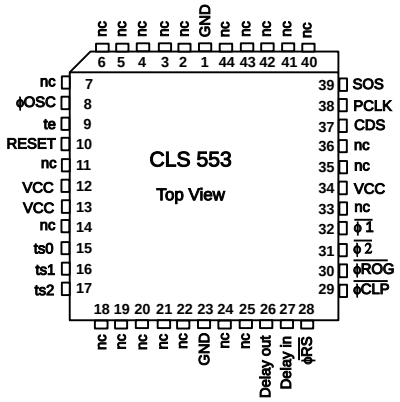
CLS 553

ccd linescan controller



Key Features:

- CCD Linescan controller
- Designed for Sony ILX 553A
- All clock signals included.
- Start of frame output.
- Selectable exposure time.

Overview:

The CLS 553 is an easy to use, complete ccd linescan controller, designed for the SONY ILX 553A linescan sensor.

For operation the CLS 553 requires power +5 V only, and a 8 MHz TTL or CMOS clock input signal. Only clock drivers are required.

To provide more flexibility, the CLS 553 has an interface to control exposure time. All inputs are connected to internal pull up resistors, so they can left unconnected if not required.

Interface:

The CLS 554 linescan controller includes all CCD-timing signals including pixel clock and exposure control.

The digital interface provides user selectable pixel clock and exposure time. An output for pixel clock and start of frame facilitates the operation with an additional frame grabber.

With an additional oscilloscope, drivers and a Sony IILX 553A CCD-sensor the CLS 553 converts to a complete very low cost CCD-linescan camera with display. (See the application on the last page).

khs instruments

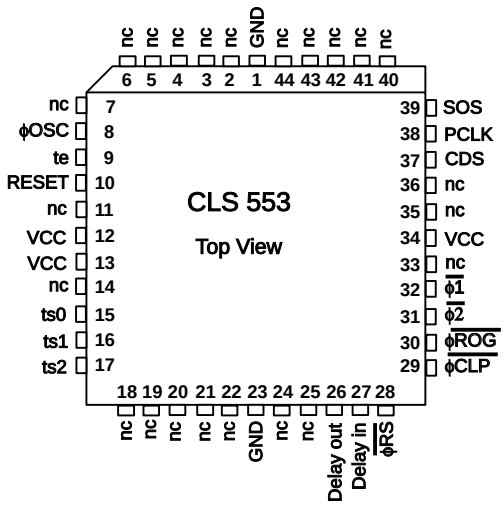
Absolute Maximum Ratings

VCC Supply voltage	- 0.5 V to + 6 V
Input voltage applied	- 0.5 to Vcc + 0.5 V
Digital output current	0 to 5 mA
Storage temperature	- 20 to 150 °C
Operating temperature	0 to 50 °C

DC Characteristics

Output low voltage (8 mA)	0.4V
Output high voltage (-4 mA)	2.4V
Input pullup current	-0.15 mA
Input low Voltage (max)	0.8 V
Input high voltage (min)	2.0V
Power requirements:	+5V 200mA

Pin Configuration



44-Pin PLCC Pinout Diagram

User Interface

Connections:

Signal	Pin	Pin	Signal
SOS	39	10	Reset
PCLK	38	8	ϕOSC
CDS	37		
ts2	17	27	Delay in
ts1	16	28	Delay out
ts0	15		
te	9		

All inputs: 50 K pull up to VCC.

Pinout description:

Pin Name	Pin Type	Pin Description
SOS	OUT	Start of scan output, low active.
PCLK	OUT	Pixelclock output, low active.
CDS	OUT	Clock for correlated doublesampling, low active.
ts0..ts1	IN	Exposure control.
te	IN	Exposure control external.
ϕOSC	IN	Oscillator input
Reset	IN	CCD asynchron reset low active
Delay in	IN	Clock delay must be connected to Delay out
Delay out	OUT	Clock delay must be connected to Delay in
nc	NC	Do not connect!

CCD Interface

Connections:

Signal	Pin
ϕ1 ϕ2	31, 32
ϕROG	30
ϕCLP	29
ϕRS	28

Pinout description:

Pin Name	Pin Type	Pin Description
ϕCLK	OUT	Inverted Clock pulses
ϕROG	OUT	Inverted Clock pulse
ϕCLP	OUT	Inverted Clock pulse
ϕRS	OUT	Inverted Clockpulse

Power

Connections:

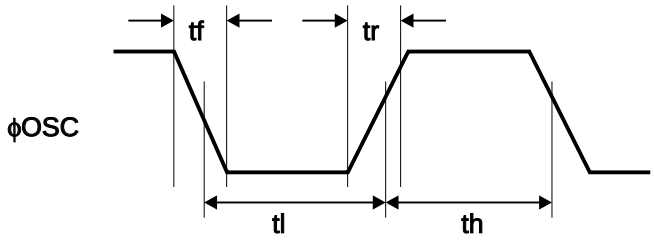
Signal	Pin
GND	1
GND	23
VCC	12
VCC	13
VCC	34

Pinout description:

Pin Name	Pin Type	Pin Description
GND	Power	Power Ground.
VCC	Power	Power + 5 V.

CLS 553

ϕOsc Timing



Item	Symbol	Min.	Typ.	Max.	Unit
ϕOSC pulse Duty *1	-	-	50	-	%
ϕOSC pulse rise / fall time	tr, tf	0	10	20	ns
ϕOSC frequency	-	-	8	48	MHz

*1 100 x th / (tl + th)

Exposure timer control

ts2	ts1	ts0	exposure time
1	1	1	22528 τ
1	1	0	32768 τ
1	0	1	65536 τ
1	0	0	131072 τ
0	1	1	do nou use
0	1	0	do not use
0	0	0	extern

Note) τ is the period of ϕCLK (τ = 500 ns at 8 MHz).

CLS 553

Application

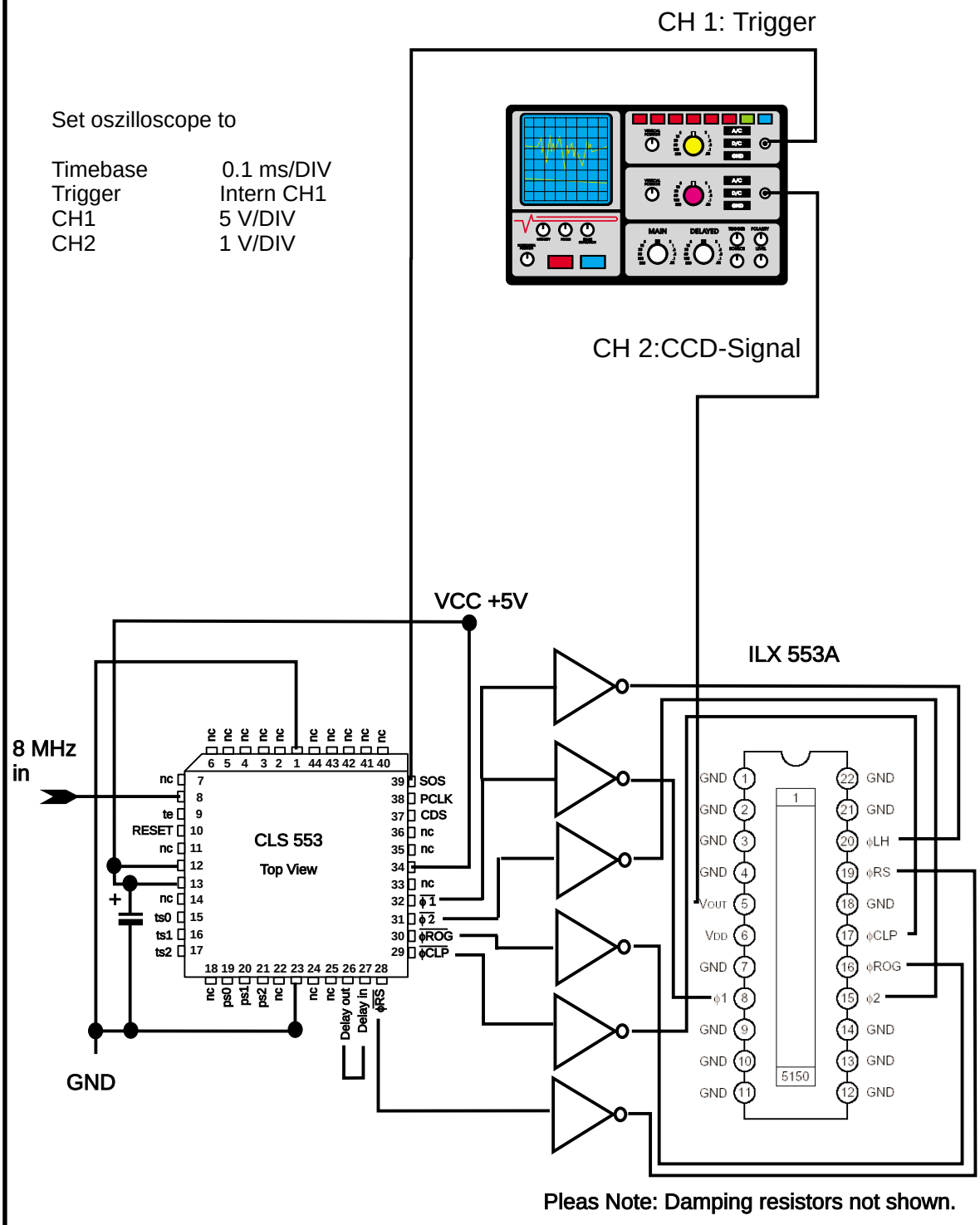


Fig. 1 Simplified Test Circuit

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